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EXAMINER	
LEGESSE, HENOK D	

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2861	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/577,320	HIRAYAMA, NOBUYUKI	
	Examiner	Art Unit	
	Henok Legesse	2861	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-26 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-26 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *See Continuation Sheet*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Continuation of Attachment(s) 3). Information Disclosure Statement(s) (PTO/SB/08), Paper No(s)/Mail Date :04/28/06,07/20/06,8/4/06,9/29/06,1/9/07,&2/5/07.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1, 2, 4, 6-9, 11-15, 18, 19, 21, 23, and 24 rejected under 35 U.S.C. 102(b) as being anticipated by Nagumo (US 6,400,349).

Regarding claims 1 and 14, Nagumo teaches a printhead (thermal printer, col.1, lines 7-9; Note that thermal printer inherently has a printhead and printhead of a thermal printer inherently has plurality of printing elements, heaters, arranged on a printhead substrate) having a plurality of printing elements (heating elements, col.1, lines 7-9), comprising:

a plurality of switching elements (M2 in fig.2; Note that there is at least one switching transistors M2 in each of the driving circuits 208 in fig.1) being arranged in correspondence with the respective printing elements (heating elements, col.1, lines 7-9; Note that the driving circuits 208 in figs.1, 2 can be used to drive a heating elements of a thermal printer, col.1, lines 5-10, but in figs.1, 2, 208 is shown as an LED driver) and configured to control energization to the respective printing elements (heating elements of thermal printer);

a reference voltage circuit (203 fig.1) configured to generate a reference voltage (V_{REF} fig.2);

a current generation circuit (R_{ref}, 100, 101,V_{REF}, fig.2) configured to generate a reference current (I_{ref}) on the basis of the reference voltage (V_{REF}) generated by said reference voltage circuit (203 fig.1); and

a plurality of constant current sources (M1 in fig.2; Note that there is at least one constant current source M1 in each of the driving circuits 208 in fig.1) configured to supply, in accordance with the reference current (I_{ref}) generated by said current generation circuit (R_{ref}, 100, V_{REF} fig.2), constant currents (I_{D1}) via said switching elements (M2) arranged in correspondence with the respective printing elements (heating elements of thermal printer) (figs.1,2;col.1, lines 5-10, col.7, lines 10-63, col.8, lines 15-63).

Regarding claims 2,9,15, and 21, Nagumo further teaches the respective constant current sources (M1,... in fig.2) form current mirror circuits with current output circuit portions of said current generation circuit (constant current source M1 forms a current mirror circuit with 101, see fig.2; col.8, lines 40-44).

Regarding claims 4 and 11, Nagumo further teaches the printing element (heating elements of a thermal printer, col.1, lines 7-9), said switching element (M2,... in fig.2), and said constant current source (M1,...) are series-connected (see fig.2; Note that in fig.2 the driving circuit 208 is used to drive LED however the same driving circuit

208 can be used to drive the heating element of a thermal heater by replacing the LED with heating elements. col.1, lines 5-10).

Regarding claims 7,13,19 and 24, Nagumo further teaches the printing elements (heating elements of a thermal printer, col.1, lines 7-9), the switching element (M2,... in fig.2) and the constant current source (M1,...) are connected in series between a high voltage wiring (power supply line,V_{DD}) and a low voltage wiring (ground line) in an order of the printing elements (heating elements replaces LED in fig.2), the switching element (M2) and the constant current source (M1) (see fig.2).

Regarding claims 8 and 20, Nagumo teaches a printhead (thermal printer, col.1, lines 7-9; Note that thermal printer inherently has a printhead and printhead of a thermal printer inherently has plurality of printing elements, heaters, arranged on a printhead substrate) comprising:

a plurality of element driving blocks (208,fig.1; Note that driver circuit 208 is also used to drive heating elements in a thermal printer see.col.1, lines 7-9) each having a plurality of printing elements (heating elements, col.1, lines 7-9 also figs.1, 2), a plurality of switching elements (M2 in fig.2;Note that there is at least one switching transistors M2 in each of the driving circuits 208 in fig.1) configured to be arranged in correspondence with the respective printing elements (heating elements of thermal printer) and control energization to the respective printing elements (heating elements of thermal printer), and a plurality of constant current sources (M1 in fig.2; Note that there

is at least one constant current source M1 in each of the driving circuits 208 in fig.1) configured to supply constant currents via said switching elements (M2,... in fig.2) arranged in correspondence with the respective printing elements (heating elements of thermal printer);

a reference voltage circuit (203 fig.1) configured to generate a reference voltage(V_{REF} fig.2); and

a current generation circuit (R_{ref}, 100, 101,V_{REF}, fig.2) configured to generate a plurality of reference currents (I_{ref}) on the basis of the reference voltage (V_{REF}) generated by said reference voltage circuit (203 fig.1) (see fig.1 there are plurality of driver circuits 208),

wherein each of the constant current sources (M1 in fig.2; Note that there is at least one constant current source M1 in each of the driving circuits 208 in fig.1) being arranged in each of said plurality of element driving blocks (208 in fig.1) supplies a constant current (I_{D1}) corresponding to any one of the plurality of reference currents (I_{ref}) via said switching element (M2,...) being arranged in correspondence with the each printing element (heating elements of thermal printer) of said element driving block (208) (figs.1,2;col.1, lines 5-10, col.7, lines 10-63, col.8, lines 15-63).

Regarding claims 6,12,18, and 23, Nagumo further teaches said constant current source (M1 in fig.2) is formed using MOS transistors (see fig.2), each of which operates in a saturation region wherein a drain current hardly changes with respect to a drain voltage (fig.8 and col.8,lines 44-48).

3. Claims 1, 2, 4, 7-9, 11, 13-15, 19-21, and 24-26 rejected under 35 U.S.C. 102(b) as being anticipated by Matsuno Yasushi (JP Pub.# 2000-246900).

Regarding claims 1 and 14, Matsuno teaches a printhead (IJH, Ink Jet Head in fig.4; Note that the printhead inherently has a printhead substrate where the plurality of heater elements are arranged) having a plurality of printing elements (heater elements, RH, RH1, RH2,...), comprising:

a plurality of switching elements (S1A,S1B,S2A,S2B,.... fig.12) being arranged in correspondence with the respective printing elements (RH1, RH2,...) and configured to control energization to the respective printing elements (RH1, RH2,...);

a reference voltage circuit configured to generate a reference voltage (VDD fig.12; inherently there is a circuit that supplies VDD);

a current generation circuit (101,102,M1) configured to generate a reference current (I_{ref1},I_{ref2}) on the basis of the reference voltage (VDD) generated by said reference voltage circuit; and

a plurality of constant current sources (M2.M3,...) configured to supply, in accordance with the reference current (I_{ref1},I_{ref2}) generated by said current generation circuit (101,102,M1), constant currents via said switching elements (S1B,S2B,....) arranged in correspondence with the respective printing elements (RH1, RH2,...).

Regarding claims 2,9,15, and 21, Matsuno further teaches the respective constant current sources (M2.M3,...) form current mirror circuits with current output

circuit portions of said current generation circuit (constant current sources M2 and M3 forms a current mirror circuit with M1, see fig.12).

Regarding claims 4 and 11, Matsuno further teaches the printing element (RH1, RH2,... fig.12) , said switching element (S1B,S2B,....), and said constant current source(M2.M3,...) are series-connected (see fig.12).

Regarding claims 7,13,19 and 24, Matsuno further teaches the printing elements (RH,RH1, RH2,... fig.12,9), the switching element (S1,S2,S3,S1B,S2B,....) and the constant current source (I1,I2,I3,M2.M3,...) are connected in series between a high voltage wiring (power supply line) and a low voltage wiring (ground line) in an order of the printing elements, the switching element and the constant current source (see fig.9 and 12) (Note that in a seriously connected elements, the order of the elements connected inherently does not have any effect in the characteristics of the circuit).

Regarding claims 25 and 26, Matsuno further teaches a printhead (IJH, inkjet head fig.4) defined in claim 1(see figs. 4,12 and claim 1 rejection above);

and an ink tank (IJC, inkjet cartridge in fig.4) configured to accommodate ink to be supplied to said printhead (IJH),

and driving means (1705 in fig.5;302 in fig.13;300 in figs.10-12) for driving said printhead in accordance with a printing signal.

Regarding claims 8 and 20, Matsuno teaches a printhead (IJH, Ink Jet Head in fig.4; Note that the printhead inherently has a printhead substrate where the plurality of heater elements are arranged) comprising:

a plurality of element driving blocks (printing elements, heater, driving circuits in figs.5,10-12,) each having a plurality of printing elements (heater elements, RH, RH1, RH2,... figs.4,12), a plurality of switching elements (S1A,S1B,S2A,S2B,.... fig.12) configured to be arranged in correspondence with the respective printing elements (RH1, RH2,...) and control energization to the respective printing elements (RH1, RH2,...), and a plurality of constant current sources (M2.M3,...) configured to supply constant currents via said switching elements (S1B,S2B,....) arranged in correspondence with the respective printing elements (RH1, RH2,...);

a reference voltage circuit configured to generate a reference voltage (VDD fig.12; inherently there is a circuit that supplies VDD); and

a current generation circuit (101,102,M1) configured to generate a plurality of reference currents (I_{ref1},I_{ref2}) on the basis of the reference voltage (VDD) generated by said reference voltage circuit,

wherein each of the constant current sources (M2.M3,...) being arranged in each of said plurality of element driving blocks (printing elements, heater, driving circuits) supplies a constant current corresponding to any one of the plurality of reference currents (I_{ref1},I_{ref2}) via said switching element (S1B,S2B,....) being arranged in correspondence with the each printing element (RH1, RH2,...) of said element driving block.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 3,10,16, and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Matsuno Yasushi in view of Okada et al (US 5,866,713).

Regarding claims 3,10,16,and 22, Matsuno teaches substantially teaches the claimed invention except for the plurality of printing elements and said plurality of switching elements are divided into a plurality of groups, and the respective constant current sources are connected to the respective groups.

However, from the same endeavor Okada et al teaches grouping of plurality of printing elements and plurality of switching elements into a plurality of groups (see fig. 11; col.2, lines 36-67, col.3, lines 1-26).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to group plurality of printing elements and plurality of switching elements of Matsuno in to a plurality of groups as taught by Okada et al in such away that the respective constant current sources of Matsuno are connected to

the respective groups. The motivation being since in this arrangement fewer heaters are simultaneously driven in each group during printing, over heating of a print head is suppressed. Thus high quality printing image is obtained (see col.2, lines 52-55 of Okada et al).

6. Claims 5 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Matsuno Yasushi in view of Yaklin (US 2003/0038617).

Regarding claims 5 and 17, Matsuno teaches substantially teaches the claimed invention except for the reference voltage circuit generates as the reference voltage a voltage obtained by amplifying a band gap voltage.

However, Yaklin teaches a reference voltage circuit (220,224 in fig.6) that generates a reference voltage (234) obtained by amplifying a band gap voltage (V_{BG}).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to utilize the reference voltage circuit of Yaklin in the circuit of Matsuno to provide a more stable reference voltage VDD.

7. Claims 6, 12, 18, and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Matsuno Yasushi in view of Nagumo (US 6,400,349).

Regarding claims 6, 12, 18, and 23, Matsuno teaches substantially teaches the claimed invention, constant current source (M2.M3,... fig.12) is formed using MOS

transistors. But fails to expressly teach the constant current sources (M2.M3,...) operates in a saturation region wherein a drain current hardly changes with respect to a drain voltage.

However, Nagumo teaches constant current source (M 1,fig.2) formed using MOS transistors that operates in a saturation region (col.8,lines 44-48) wherein a drain current hardly changes with respect to a drain voltage (fig.8 and col.8,lines 44-48).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to operate the constant current source (M2.M3,... fig.12) of Matsuno in a saturation region based on the teaching of Nagumo in order to make the constant current from the constant current substantially constant, regardless of variations in the power supply or ground potential thereby resulting in better image quality (fig.8 and col.8, lines 44-48).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Henok Legesse whose telephone number is (571)270-1615. The examiner can normally be reached on Mon - FRI, 7:30-5:00, ALT.FRI EST.TIME.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Luu can be reached on (571) 272-7663. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

*** H.L. 08/06/2008

MATTHEW LUU
SUPERVISORY PATENT EXAMINER